UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,106	06/12/2001	Tim Allen	ALTRP064	3098

22434 7590 02/16/2005

BEYER WEAVER & THOMAS LLP
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,106	ALLEN ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-23 and 25-93* is/are pending in the application.

4a) Of the above claim(s) *32-93* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-23 and 25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 09/880,106 and amendment filed on 1/25/2005. Claims 1-12, 14-23 and 25-31 are pending, claims 13 and 24 are canceled, and claims 32-93 are withdrawn from consideration.

2. The finality of the action on 12/22/2004 is withdrawn due new ground of rejections as followed.

Claim Objections

3. Claims 15 and 31 are objected to because of the following informalities: claim 15, line 1, "claim 1" should be changed to --claim 14-- in order to provide proper claim dependency and claim 31, phrase "The system of claim 18," should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-12, 14-15, 18-23 and 25-31 are rejected under 35 U.S.C. 103(a) as being obvious over Gosior et al. (US 2003/0093655) in view of Sharma et al. (5,841,663).

6. As to claims 1, 18, 25 and 31, Gosior et al. teach implementing a programmable chip (a processor core and peripherals embedded on a single programmable chip). The

programmable single chip includes a processor core that that be configured according to a parameter information (a first parameter) (Fig. 1, processor core 12, at least in [0024, 0028, 0029, 0048]), and peripherals that also can be configured according to a parameter information (a second parameter) (Fig. 1, supervisory control unit, peripheral adapter, peripheral interface devices; at least in [0020, 0022, 0023, 0024, 0026, 0027, 0039, 0048]). Thus, Gosior et al. a programmable chip comprises a parameterized processor core and parameterized peripherals, where the parameters can be modified according to desired applications. Gosior et al. also teach the peripherals include peripheral adapter logic (device driver logic) (see Fig. 2, [0039]). Also noted that the device driver logic is inherent within the peripheral device. Gosior et al. do not explicitly teach generating a logic description for implementing the processor core and peripherals on the programmable chip. But the act of generating a logic description for implementing any IC design using parameters is well known to one practitioner in IC design art. The act of generating the logic description for implementing an IC design based on parameterized modules is described in Sharma's patent (at least see summary). Therefore, in order to implementing the processor core and peripherals using parameters information as taught by Gosior et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a logic description using the first and second parameters in order to provide logic information (a synthesized netlist as described in the patent to Sharma et al.), where the logic information comprising device driver logic information for implementing the peripheral on the programmable chip.

7. As to claims 2-6, 19-20, 26 and 27, Gosior et al. teach the peripheral is a peripheral component (Fig. 1-2); the peripheral component is a parameterizable peripheral component available from a library of peripherals that includes a plurality of parameterizable peripherals, the peripheral is a peripheral interface, wherein the peripheral is an interface to off-chip memory (Fig. 1-2, 0024, 0025, 0026, 0027, 0038, 0039, 0048]). It is noted that a library or database must be used to store circuit elements. This is a common practice in IC design. Thus, since Gosior et al. a programmable chip architecture comprising a plurality of peripherals (a group of peripheral, various generic interface devices to implemented with a processor core on the programmable chip, 0026, 0028), thus in order to implement a peripheral, the peripheral must be selected from a group of peripherals stored in a library. In addition, Sharma et al. also teach a parameterized HDL library module that is composed of one or more parameterized HDL modules that can be to customize programmable logic device by changing parameter values (see summary).

8. As to claims 7-10, 21-22 and 28-29, Sharma et al. teach generating a logic description that is a synthesized/synthesizable netlist (synthesized logic file), an HDL file. It is noticed that use an EDIF file (EDF file) to describe the logic description is known to one practitioner in IC design.

9. As to claims 11-12, 23 and 30, Gosior et al. teach the single programmable chip embedded processor core with peripherals that are used to interface to external systems. The system is used for various embedded input/output applications such as baseband processor unit connected to a RF transceiver for communications

applications and as an embedded device controller (0001, 0010, 0022, 0024, 0025). Thus these peripherals are customized according to communications applications.

10. As to claims 14-15, Gosior et al. teach a single programmable chip comprising a processor core interconnecting to a plurality of peripherals to interface to external systems. This clearly suggests having connector logic for allowing interconnection between the processor core and the peripheral(s) in order to identify I/O ports associated with processor core and the peripheral(s). In addition, Sharma et al. also teach designing g an IC using parameterized HDL modules, where the parameterized modules include an entity description, a behavioral description and implementation description, where the entity description specifies the parameters, input/output ports for a circuit element available in HDL library (see summary). Therefore, the teachings of Gosior et al. alone, or a combination of teachings with Sharma et al. would rendered the claims obvious to one of practitioner in IC design art in order to generate a synthesized netlist including all necessary information that can be used to implement the single programmable chip.

11. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Gosior et al. (US 2003/0093655) in view of Sharma et al. (5,841,663) in further view of Gauthier et al. (6,574,791).

12. As to claims 16-17, Gosior et al. and Sharma et al. do not explicitly teach wizards and subwizards. Gauthier et al. teach a component based wizard creation mechanism that provides an environment and set facilities for creating and modifying wizards by providing a WizardWizard mechanism for creating the skeleton of new wizard, a

WizardDesigner mechanism for specializing and WizardMetaDataManager mechanism for persisting and retrieving created wizards. The WizardWizard guides the developer through a predetermined series of steps that are required to define the basic components of a new wizard. The WizardDesigner take these basic components and guides the developer through a specialization process that further customizes and defines the new wizard. Also the WizardWizard and the WizardDesigner create and specialize the target wizard from a component based framework to provide a customized and extendable wizard and creation solution to that has utmost functionality and flexibility to users and developer (col. 2, lines 45-65; col. 6 line 47 to col. 7 line 58). Fig. 11-28 show and describe wizards and subwizards. With all these motivations, it would been obvious to one of ordinary in the art at the time the invention was made to have provided the first parameter and second parameter information through a wizard and a subwizard, where the subwizard spawned as a result of user interaction with the wizard in order to create new target programmable chip by modifying the parameters as desired to thereby customize the programmable chip according to applications as needed.

13. Claims 1-12, 14-15, 18-23 and 25-31 are rejected under 35 U.S.C. 103(a) as being anticipated by Rhim et al. (6,006,022) in view of Sharma et al. (5,841,663).

14. As to claims 1, 18, 25 and 31, Rhim et al. teach a method for implementing a programmable chip comprising identifying first parameter information for configuring the processor core on the programmable chip; identifying second parameter information for configuring the peripheral on the programmable chip and generating a logic description

using the first and second parameter information to provide logic information for implementing the processor core and the peripheral on the programmable chip (Fig. 1 and description; col. 14-16, summary). Notice that device driver logic is art inherent within the peripherals. Rhim et al. do not explicitly teach generating a logic description based on parameters for implementing an IC design. But the act of generating a logic description for implementing any IC design using parameters is well known to one practitioner in IC design art. Such act of generating the logic description for implementing an IC design based on parameterized modules is described in Sharma's patent (at least see summary). Therefore, in order to implementing the processor core and peripherals using parameters information as taught by Rhim et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a logic description using the first and second parameters in order to provide logic information (a synthesized netlist as described in the patent to Sharma et al.), where the logic information comprising device driver logic information for implementing the peripheral on the programmable chip.

15. As to claims 2, 5-12, 14-15, 19-23 and 26-30, Rhim et al. teach the peripheral is a peripheral component; a peripheral interface, a custom peripheral interface and an interface to off-chip (external device); the logic description is a synthesizable logic file, an HDL file, EDF file; the logic description comprises generating connector logic for allowing interconnects between the processor core and the peripheral; generating connector logic comprising identifying the I/O ports associated with the processor core and the peripherals (Fig. 1 and description; col. 14-18, summary).

16. As to claims 3-4, Sharma et al. teach a design database that is known to be used to store design information relating to developing and producing a field programmable system, where the field programmable includes processor core and peripherals. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to recognize that the design database is used to store design information including peripherals (parameterizable peripherals since the field programmable system or device as taught by Rhim et al. can be reprogrammed and models are based on parameters that can be modified, at least see Fig. 6 and its description).

17. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Rhim et al. (6,006,022) in view of Gauthier et al. (6,574,791).

18. As to claims 16-17, Rhim et al does not teach wizard and subwizard. Gauthier et al. teach an object oriented wizard creation mechanism including a WizardDesigner mechanism for creating skeleton of new wizard, for specializing, and WizardMetaManager mechanism for persisting and retrieving created wizards. The WizardWizard guides the developer to define basic components of new wizard. The use of the component based framework with the WizardWizard and WizardDesigner provide a customizable and extensible wizard creation solution to that has utmost functionality and flexibility to the users and developers (please at least col. 2, col. 4, lines 26-41, col. 7, 9-10). Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to utilizing the object oriented wizard creation mechanism as taught by Gauthier et al. during implementing the programmable chip as

taught by Rhim et al. in order to customize the programmable chip including a core processor an peripheral by modifying parameter information of the core processor and peripheral to thereby providing various functionality of the programmable chip.

Remarks

19. Examiner respectively submits that the allowable subject matter to claims 13 and 24 are withdrawn in view of new ground of rejection. The generating a logic description information including device driver logic information for implementing the peripheral on the programmable chip is not novel. The device driver logic information is included within the peripheral device logic as taught by Gosior or Rhim. In order to implementing a programmable chip/programmable device/programmable system including the processor core and peripherals, a logic description information must be generated and since the programmable chip can be modified or reprogrammed based on parameters, the logic description information must be included information relating to processor core and peripherals (device driver logic). Accordingly, the claims are not patentable.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER